remaining processing steps includes gate oxidation to form the gate oxide, forming the gate electrode and forming the N+ and P+ diffusion regions.

[0028] In alternate embodiments of the present invention, the deep diffusion region can be formed using a multiple epitaxial layer process instead of high energy implantation. Thus, the epitaxial layer is formed to a first thickness and then an implantation step is performed to form the deep diffusion region. Then, the remaining portion of the epitaxial layer may be formed. In this manner, the deep diffusion region is formed buried in the epitaxial at a depth deeper than the P-body region to be formed. In other embodiments, multiple epitaxial and implantation process can be performed to form a graded doping profile at the deep diffusion region.

[0029] In the above description, the JFET device and the LDMOS transistor device are both N-type devices. One of ordinary skill in the art would appreciate that P-type JFET device and P-type LDMOS transistor can be formed using semiconductor material and diffusion regions of the opposite polarity types.

[0030] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, the invention is not limited to the details provided. There are many alternative ways of implementing the invention. The disclosed embodiments are illustrative and not restrictive.

What is claimed is:

1. A power integrated circuit, comprising:

a semiconductor layer of a first conductivity type and being lightly doped;

a junction field effect transistor (JFET) device formed in a first portion of the semiconductor layer and being formed in a first deep well of a second conductivity type, the JFET device including a gate region formed using a first body region of the first conductivity type, source and drain regions of the second conductivity type formed on opposite sides of the gate region, a channel of the JFET device being formed in an area of the first deep well between the source region and the drain region outside of the gate region;

a double-diffused metal-oxide-semiconductor (LDMOS) transistor formed in a second portion of the semiconductor layer and being formed in a second deep well of the second conductivity type, the LDMOS transistor including a second body region of the first conductivity type formed in the second deep well, a gate electrode, a source region, and a drain drift region in electrical contact with a drain region, a channel of the LDMOS transistor being formed in the second body region between the source region and the drain drift region, wherein the second body region is formed to optimize a threshold voltage and a breakdown voltage of the LDMOS transistor and the first and second body regions have the same doping concentration and depth;

a first deep diffusion region formed in the first deep well under the first body region and in electrical contact with the first body region, the first deep diffusion region together with the first body region establishing a pinch off voltage of the JFET device; and

a second deep diffusion region formed in the second deep well under the second body region and in electrical contact with the second body region, the second deep diffusion region forming a reduced surface field (RESURF) structure in the LDMOS transistor.

2. The power integrated circuit of claim **1**, wherein the LDMOS transistor further comprises:

the gate electrode being formed partially overlapping the body region and insulated from the semiconductor body by a gate dielectric layer;

the source region of the second conductivity type being formed in the second body region on a first side of the gate electrode; and

the drain drift region of the first conductivity type being formed in the second deep well; and

a drain region being formed in the drain drift region, the drain region comprising a first well of the second conductivity type.

3. The power integrated circuit of claim **1**, wherein the semiconductor layer comprises:

a semiconductor substrate of the first conductivity type; and

an epitaxial layer of the first conductivity type formed on the semiconductor substrate.

4. The power integrated circuit of claim **1**, wherein the first and second body regions are formed using the same processing steps including using the same implant dose and the same implant energy, the implant dose and the implant energy being selected to optimize a threshold voltage and a breakdown voltage of the LDMOS transistor.

5. The power integrated circuit of claim **1**, wherein the first and second deep diffusion regions are formed using the same processing steps and have the same doping concentration and depth, the first and second deep diffusion regions being more heavily doped than the first and second body regions.

6. The power integrated circuit of claim **5**, wherein the first and second deep diffusion regions have a graded doping profile, the doping concentration decreasing from a first edge of the first or second deep diffusion region near the respective body region to a second edge away from the respective body region.

7. The power integrated circuit of claim **1**, wherein the first deep diffusion region has a width that is coincidence with the first body region or extends beyond the first body region on both sides of the first body region.

8. The power integrated circuit of claim **7**, wherein the first deep diffusion region is spaced apart from the drain region by a first distance and is spaced apart from the source region by a second distance, the first distance being greater than the second distance.

9. The power integrated circuit of claim **1**, wherein the second deep diffusion region has a width that is coincidence with the second body region or extends beyond the second body region towards the drain drift region or extends under the drain drift region.

10. The power integrated circuit of claim **1**, wherein the first conductivity type is P-type and the second conductivity type is N-type.

11. The power integrated circuit of claim **3**, further comprising:

a first buried layer of the first conductivity type formed in the first portion of the semiconductor layer between the epitaxial layer and the semiconductor substrate; and

a second buried layer of the second conductivity type formed in the second portion of the semiconductor layer between the epitaxial layer and the semiconductor substrate.

12. A method for forming a power integrated circuit, comprising: